

avr risc microcontroller handbook pdf

A reduced instruction set computer, or RISC (/ r Éª s k /), is one whose instruction set architecture (ISA) allows it to have fewer cycles per instruction (CPI) than a complex instruction set computer (CISC). Various suggestions have been made regarding a precise definition of RISC, but the general concept is that such a computer has a small ...

Reduced instruction set computer - Wikipedia

MIPS (an acronym for Microprocessor without Interlocked Pipelined Stages) is a reduced instruction set computer (RISC) instruction set architecture (ISA): A-1: 19 developed by MIPS Technologies (formerly MIPS Computer Systems).

MIPS architecture - Wikipedia

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